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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/624,321	07/24/2000	Bing-Chang Wu	8693-000221	6623

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EXAMINER

LUU, CHUONG A

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/624,321

Applicant(s)

WU, BING-CHANG

Examiner

Chuong A. Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 March 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) 9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election without traverse of Group I, claims 1-8 in the reply filed on March 12, 2003 is acknowledged.

### ***Claim Objections***

Claims 1-8 are objected to because of the following informalities: In claim 1, line 12, "pattering" is misspelled; it should be --patterning--. Appropriate correction is required.

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

### **The Rejections**

Claims 1-2 and 5-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U.S. 6,399,476 B2).

Kim discloses a semiconductor device with

(1) providing a substrate (100) having a plurality of semiconductor elements (106) and one dielectric layer (106) for isolating the semiconductor elements (106) formed thereon (see Figure 2);

forming a metal layer (106) over said substrate (100);

forming a pad oxide layer (108) over said metal layer (106);

patterning and etching said pad oxide layer (108) and metal layer (106) to constitute said interconnect lines over said substrate (100) (see Figure 2);

forming an inter-metal dielectric layer (112, 116) over said substrate (100) having said interconnect lines (106) formed thereon, wherein at least an air gap (114) is formed in a spacing between the adjacent interconnect lines (106) (see Figures 3-4);

planarizing said inter-metal dielectric layer (112, 116) (see column 5, lines 29-34);

(2) wherein said metal layer is formed from materials selected from the group consisting of Al (see column 4, lines 35-45);

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(5) wherein said pad oxide layer comprises SiO<sub>2</sub>, deposited by plasma enhanced CVD method (see column 4, lines 50-62);

(6) wherein said inter-metal dielectric layer comprises a SiO<sub>2</sub> layer, deposited by plasma enhanced CVD method, utilizing TEOS/O<sub>3</sub> as reaction gas (see column 4, lines 8-62).

### **PRIOR ART REJECTIONS**

#### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

#### **The Rejections**

Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. 6,399,476 B2).

Kim does not explicitly disclose the thickness of said pad oxide layer is between about 2000 Å and about 5000 Å; the inter-metal dielectric layer comprises a BPSG layer, deposited by plasma enhanced CVD method, utilizing TEOS, O<sub>3</sub>/O<sub>2</sub>, TMP and TMB as reaction gas, at temperature between about 400°C and 500°C. However, the thickness of said pad oxide layer is between about 2000 Å and about 5000 Å; the inter-metal dielectric layer comprises a BPSG layer, deposited by plasma enhanced CVD method, utilizing TEOS, O<sub>3</sub>/O<sub>2</sub>, TMP and TMB as reaction gas, at temperature

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between about 400°C and 500°C is considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the thickness of said pad oxide layer is between about 2000 Å and about 5000 Å; the inter-metal dielectric layer comprises a BPSG layer, deposited by plasma enhanced CVD method, utilizing TEOS, O<sub>3</sub>/O<sub>2</sub>, TMP and TMB as reaction gas, at temperature between about 400°C and 500°C of Kim's device within the range as claimed for the purpose of obtaining the better performance, and it also has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP j 2144.05).

Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. 6,399,476 B2) in view of Lin et al. (U.S. 6,211,057 B1).

Kim teaches the above outlined features except for wherein said pad oxide layer comprises SiO<sub>2</sub>, deposited by atmospheric pressure CVD method; wherein said inter-metal to dielectric layer comprises a BPSG layer, deposited by atmospheric pressure CVD method, utilizing TEOS/O<sub>3</sub>, TMPO and TEB as reaction gas, at temperature lower than 550°C. Lin discloses a semiconductor device with (4) wherein said pad oxide layer comprises SiO<sub>2</sub>, deposited by atmospheric pressure CVD method (see column 3, lines 56-57); (7) wherein said inter-metal to dielectric layer comprises a BPSG layer, deposited by atmospheric pressure CVD method, utilizing TEOS/O<sub>3</sub>, TMPO

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and TEB as reaction gas, at temperature lower than 550°C (see column 3, lines 56-59). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kim (accordance with the teaching of Lin). Doing so would facilitate the manufacture of the semiconductor structure and increase the speed of the semiconductor device.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong Anh Luu  
Patent Examiner  
April 4, 2005